B1 C1

1. (Amended) Apparatus for tightly-coupling hardware data encryption functions with software-based protocol decode processing within a pipelined processor of a programmable processing engine in a network switch, the apparatus comprising:

an encryption execution unit contained within the pipelined processor; and

a software and hardware interface that enables the encryption execution unit to efficiently cooperate with resources of the pipelined processor by the pipelined processor executing opcodes to control the encryption execution unit.

B2 C2

10. (Amended) A method for tightly-coupling hardware data encryption functions with software-based protocol decode processing within a pipelined processor of a programmable processing engine in a network switch, the method comprising the steps of:

providing an encryption execution unit within the pipelined processor; and

selectively accessing the encryption execution unit through an integrated hardware and software interface of the pipelined processor that allows efficient cooperation between the encryption execution unit and resources of the pipelined processor by the pipelined processor executing opcodes to control the encryption execution unit.

B3 C3

20. A programmable processing engine of a network switch comprising:

an input header buffer;

an output header buffer; and

a plurality of processing complex elements symmetrically arrayed into rows and columns that are embedded between the input header buffer and an output header buffer, each processing complex element comprising a microcontroller core having an encryption tightly coupled state machine (TCSM) unit that is selectively invoked through an integrated hardware and software interface of the microcontroller core to allow efficient cooperation between the encryption TCSM unit and data path resources of the microcontroller core by the microcontroller executing opcodes to control the TCSM.

21. (Amended) A pipelined processor in a network switch, the processor comprising:

an ALU internal to the processor responsive to a first set of opcodes;

an encryption execution unit internal to the processor having an encryption tightly coupled state machine (TCSM) responsive a second set of opcodes, and protocol processing operations are performed by the ALU and encryption operations are performed by the encryption execution unit in response to said second set of opcodes.

27. (Amended) A method for providing encryption functions within a pipelined processor in a network switch, the method comprising the steps of:

associating a first set of opcodes with an ALU internal to the processor;

B4 Cont

associating a second set of opcodes with an encryption execution unit internal to the processor having an encryption tightly coupled state machine (TCSM), and protocol processing operations are performed by the ALU and encryption operations are performed by the encryption execution unit in response to said second set of opcodes.

B5

32. (Amended) The method of Claim 27, further comprising the steps of:

performing a DES function in response to execution of a third instruction having a field containing an encryption opcode that specifies loading plaintext and initialing the DES operations.

REMARKS

This Amendment is filed in response to the Office Action mailed on July 22, 2002, and with the Continuing Prosecution Application (CPA) filed herewith. All objections and rejections are respectfully traversed.

Claims 1-34 are in the case.